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Analysis of the minority carrier response of n-type and p-type Au/Ni/Al_2O_3/$In_{0.53}Ga_{0.47}As$/InP capacitors following an optimized $(NH_4)_2S$ treatment

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Analysis of the minority carrier response of *n*-type and *p*-type Au/Ni/Al_2O_3/$In_{0.53}Ga_{0.47}As$/InP capacitors following an optimized $(NH_4)_2S$ treatment

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The electrical properties of metal-oxide-semiconductor capacitors incorporating atomic layer deposited Al_2O_3 on *n*-type and *p*-type $In_{0.53}Ga_{0.47}As$ were investigated. A clear minority carrier response was observed for both *n*-type and *p*-type Au/Ni/Al_2O_3/$In_{0.53}Ga_{0.47}As$ devices following an optimized ammonium sulfide $(NH_4)_2S$ treatment. Capacitance-voltage and conductance-voltage measurements performed at varying temperatures allowed an Arrhenius extraction of activation energies for the minority carrier response, indicating a transition from a generation-recombination regime to a diffusion controlled response. © *2011 American Institute of Physics*.
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In order to continue complementary metal oxide semiconductor (CMOS) development, III-V channel layers such as $In_{0.53}Ga_{0.47}As$, in combination with gate oxides such as Al_2O_3, are under investigation. To date, very few studies in the literature have demonstrated true minority carrier behaviour on either *n*-type or *p*-type $In_{0.53}Ga_{0.47}As$. In the case of *n*-type $In_{0.53}Ga_{0.47}As$, a capacitance voltage (CV) response at negative gate bias consistent with mid-gap interface states is typically observed, regardless of the gate oxide or passivation method employed.[1–7] In the case of *p*-type $In_{0.53}Ga_{0.47}As$, at positive gate bias, CV characteristics consistent with a mid-gap interface state response have been observed.[8–11] Recently, Trinh *et al.*[12] and Lin *et al.*[7] presented CV responses consistent with true minority carrier behaviour for *n*-$In_{0.53}Ga_{0.47}As$ and *p*-$In_{0.53}Ga_{0.47}As$, respectively. In this work, we report on a study of the minority carrier response of both *n*-type and *p*-type $In_{0.53}Ga_{0.47}As$ metal-oxide-semiconductor (MOS) devices formed using an optimized 10% ammonium sulfide ($(NH_4)_2S$) treatment.[11,13] The temperature dependent CV and GV responses are analyzed using an Arrhenius relationship to determine activation energies following the procedure described by Nicollian and Brews for SiO_2/Si devices.[14]

The $In_{0.53}Ga_{0.47}As$ epitaxial layers used in this work were either (1) ~2 μm *n*-type $In_{0.53}Ga_{0.47}As$ (S at $\sim 4\times10^{17}$ cm^{-3}) grown by metalorganic-vapour-phase-epitaxy (MOVPE) on *n*-doped (S at $\sim 2\times10^{18}$ cm^{-3}) InP(100) wafers or (2) ~2 μm *p*-type $In_{0.53}Ga_{0.47}As$ (Zn at $\sim 4\times10^{17}$ cm^{-3}) grown by MOVPE on *p*-doped (Zn at $\sim 2\times10^{18}$ cm^{-3}) InP(100) wafers. $In_{0.53}Ga_{0.47}As$ surfaces were initially rinsed for 1 min each in acetone, methanol, and isopropanol. $(NH_4)_2S$ concentrations of 10% in deionised H_2O were used (20 min, ~295 K). These optimized passivation parameters were determined from previous physical and electrical studies.[11,13] The Al_2O_3 layers (8 nm) were grown by atomic layer deposition (ALD) at 300 °C (Cambridge NanoTech, Fiji F200LLC), using alternating pulses of TMA ($Al(CH_3)_3$) and H_2O. Samples were loaded to the ALD reactor within ~3 min after removal from the $(NH_4)_2S$ solution. Finally, gate contacts ~160 nm thick were formed by e-beam evaporation of Ni (70 nm), and Au (90 nm), using a lift-off process. Electrical measurements were recorded using an Agilent E4980A and were performed on-wafer in a microchamber probe station (Cascade, Summit 12971B) in a dry air, dark environment (dew point $\leq$ 203 K).

The CV responses at room temperature (295 K) with ac signal frequencies from 20 Hz to 1 MHz for the *n*-type and *p*-type Au/Ni/Al_2O_3/$In_{0.53}Ga_{0.47}As$ devices are shown in Figs. 1(a) and 1(b), respectively. The CV response for the passivated *n*-$In_{0.53}Ga_{0.47}As$ device exhibits a small peak due to a mid-gap interface state response around -0.6 V_{gate} to -1 V_{gate}. The CV is seen to pass through this interface defect feature and then rise to a plateau over the remaining bias range, with this latter behaviour being consistent with a true minority carrier response.[14] This is in marked contrast to the frequency dispersion typically observed in the literature for

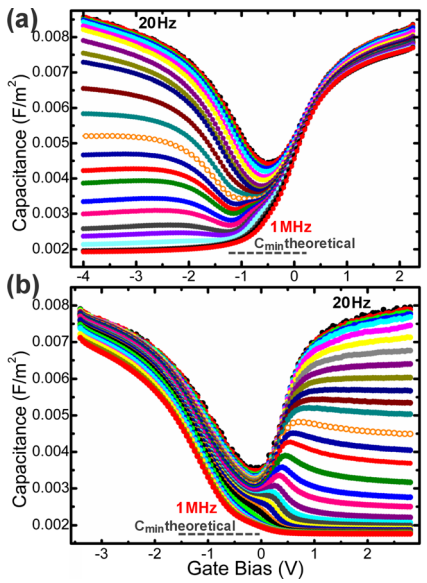

FIG. 1. (Color online) Multifrequency CV (20 Hz to 1 MHz, 295 K) for (a) *n*-type and (b) *p*-type Au/Ni/Al_2O_3/$In_{0.53}Ga_{0.47}As$ devices (optimum 10% $(NH_4)_2S$ treatment, ~3 min ALD transfer). The dispersion in accumulation is relatively low for both the *n*-type and *p*-type $In_{0.53}Ga_{0.47}As$ devices, particularly given that the measurement is over an extended frequency range of 20 Hz to 1 MHz. The theoretical C_{min} is ~0.00185 F/m^2 and 0.00182 F/m^2 for the *n*-type and *p*-type devices, respectively, calculated using the nominal $In_{0.53}Ga_{0.47}As$ doping of $\sim 4\times10^{17}$ cm^{-3}. The *p*-$In_{0.53}Ga_{0.47}As$ device received a 275 °C forming gas anneal (5% H_2:95% N_2, 30 min).

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n-type $In_{0.53}Ga_{0.47}As$,[1–7] where broad peaks associated with an interface state response are observed in the CV at negative gate bias, irrespective of the gate oxide or passivation method employed. This indicates that the mid-gap D_{it} is sufficiently low in the optimized 10% $(NH_4)_2S$ (~3 min ALD transfer time) samples analysed in this study to allow movement of the Fermi level through the mid-gap interface defect within the bias range applied. The transit time between extraction from the $(NH_4)_2S$ solution and entry to the ALD chamber is critical. For identical device structures with an increased exposure time of 7 min between the $(NH_4)_2S$ surface treatment and loading to the ALD chamber, the CV responses are dominated by a higher midgap D_{it} response,[11] and the plateau region in the CV is not observed. In the case of the *p*-type device in Fig. 1(b), the CV is also observed to pass through a peak associated with a D_{it} response before plateauing at positive gate bias, the latter being consistent with a true minority carrier response. It is also significant that the measured minimum capacitance at 1 MHz (red curves in Fig. 1(a) and 1(b)) for these *n*-type and *p*-type devices both reach the theoretical minimum capacitance. This is a strong indication that the Fermi level has been swept to the opposite band edge[8] in both cases. It is noted that the leakage current densities are low ($<6 \times 10^{-7}$ A/cm^2) over the entire bias range examined for both *n*- and *p*-type samples.

Figures 2(a) and 2(b) show G_p/ω versus ω curves for these *n*-type and *p*-type samples, respectively, obtained using the Conductance Method.[14,15] Previous work demonstrated that a D_{it} peak existed near mid-gap for similar $In_{0.53}Ga_{0.47}As$ device structures.[11] A comparable energy level was therefore chosen in order to estimate the midgap D_{it} for the samples in the current work. In the case of the *n*-type devices, the peak D_{it} at $\sim E_v + 0.4$ eV is $\sim 9 \times 10^{11}$ cm^{-2}eV^{-1}, while for the *p*-type device, the peak D_{it} at $\sim E_v + 0.4$ eV is $\sim 6 \times 10^{11}$ cm^{-2}eV^{-1}, derived using the G_p/ω curve peaks and profiles. It is important to stress that this is primarily useful here only as a qualitative estimation of the D_{it}. The minority carrier response observed for these devices renders application of conventional D_{it} extraction techniques such as the Conductance Method problematic, and makes it very difficult to accurately quantify D_{it}.[16]

The 30 kHz CV and GV responses as a function of temperature (T) for the optimized 10% $(NH_4)_2S$ passivated (~3 min ALD transfer) *n*-type $Au/Ni/Al_2O_3/In_{0.53}Ga_{0.47}As$ device are plotted in Figures 3(a) and 3(b), respectively. The CV exhibits a similar behaviour to the multi-frequency plots in Fig. 1(a). The capacitance goes through a small peak associated with a mid-gap interface state response ~ -0.6 V_{gate} before rising to a plateau over the remaining bias range. The conductance mirrors this behaviour, exhibiting a peak due to interface states in the gate bias range ~ -0.4 V to -0.8 V before rising and plateauing over the gate bias range -1.5 V to -4 V. Furthermore, this is very similar to the CV and GV behaviour versus temperature reported for a SiO_2/*n*-Si MOSCAP in inversion.[14] In particular, both the CV and GV plateau at negative gate bias. Moreover, the conductance response of the minority carriers in inversion for an MOS capacitor exhibits a specific behaviour, where at a fixed ac signal frequency, the conductance increases to a maximum value and then subsequently decreases with any further increase in temperature.[14] This characteristic is observed for the *n*-$In_{0.53}Ga_{0.47}As$ device in Figure 3(b), over the gate bias range -1.5 V to -4 V, where open symbols are used to highlight the decrease in conductance for temperatures in excess of 20 °C.

There are three possible sources of minority carriers:[14] (1) diffusion of minority carriers from the semiconductor bulk; (2) generation and recombination of minority carriers through mid-gap defects in the depletion region; (3) supply of minority carriers from an external source beyond the gate, e.g., peripheral charge induced by device processing steps. A peripheral charge effect would result in an area dependence of the minority carrier CV response and would be observed on one substrate doping polarity and not the other. In the current samples, the minority carrier response is observed over both *n*-type and *p*-type $In_{0.53}Ga_{0.47}As$ and does not vary with area, thus ruling out any contribution of peripheral or external charge effects. This leaves (1) and (2) above as the remaining sources for the minority carrier response.

The activation energy (E_A) of the minority carrier response will be half the bandgap energy (E_G) for a generation recombination process and will be equal to E_G for a diffusion controlled regime. By calculating the parallel inversion conductance (G_I), extracted from the measured conductance (G_m) and capacitance (C_m) using Eq. (1), and plotting versus 1/T, the activation energies can be obtained from the resulting Arrhenius plot.[14,16,17] G_m and C_m are taken at a V_{gate} of -4 V for the *n*-type device and at a V_{gate}

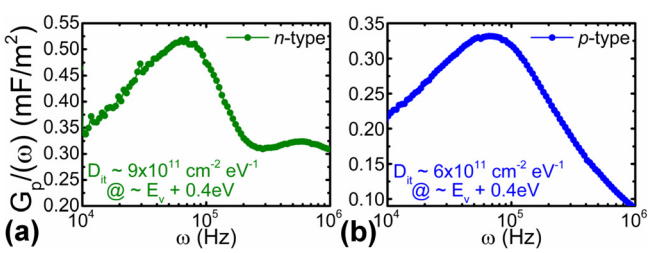

FIG. 2. (Color online) G_p/ω versus ω curves (at $V_{gate} \sim -0.6$ V, equivalent to $\sim E_v + 0.4$ eV) for (a) *n*-type and (b) *p*-type $Au/Ni/Al_2O_3/In_{0.53}Ga_{0.47}As$ devices. D_{it} was extracted from G_p/ω versus ω profiles using the Conductance Method;[14] $n = 3$; $f_D(\sigma_s) \sim 0.37$; $\xi_p(\sigma_s) \sim 2.17$.

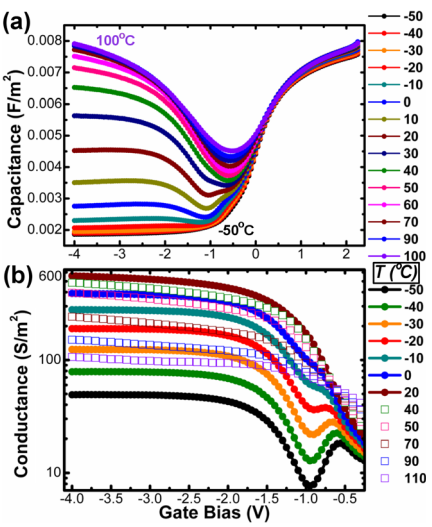

FIG. 3. (Color online) 30 kHz CV and GV responses as a function of temperature (T) (−50 °C to 110 °C), for an *n*-type $Au/Ni/Al_2O_3/In_{0.53}Ga_{0.47}As$ device (optimum 10% $(NH_4)_2S$ treatment, ~3 min ALD transfer). Open symbols are used in (b) to highlight the decrease in G_m for T > 20 °C.

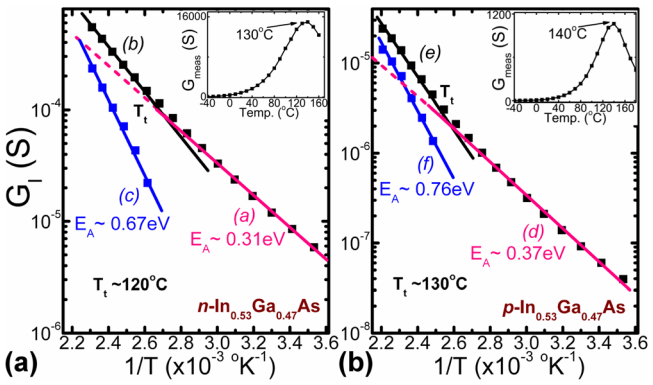

FIG. 4. (Color online) Arrhenius plots of the inversion parallel conductance (G_I) plotted versus 1/T for (a) *n*-type and (b) *p*-type Au/Ni/Al_2O_3/$In_{0.53}Ga_{0.47}As$ devices. T_t is the transition temperature. G_I was extracted at 1 MHz for the *n*-type and 60 kHz for the *p*-type device. The insets plot the measured conductance (G_m) in inversion versus T, showing that at a given frequency, the temperature where G_m peaks is approximately equal to T_t.

of 2.8 V for the *p*-type device. In the equation below, ω is the angular frequency, $\tau_o = C_{ox}/G_m$ and $\tau_m = C_m/G_m$, C_{ox} being the oxide capacitance,[14]

$$G_I = \frac{\omega^2 C_{ox}\tau_o(1+\omega^2\tau_m{}^2)}{\omega^2\tau_o{}^2 + [\omega^2\tau_m(\tau_o-\tau_m)-1]^2}. \quad (1)$$

The Arrhenius plots for the *n*-type and *p*-type $In_{0.53}Ga_{0.47}As$ devices examined in this work are shown in Figures 4(a) and 4(b), respectively. In both cases, there is a clear change in the slope of G_I versus 1/T. For the *n*-$In_{0.53}Ga_{0.47}As$ device, at lower temperature, an E_A of approximately 0.31 eV is obtained from curve (*a*), which is close to half the bandgap (~0.37 eV) for $In_{0.53}Ga_{0.47}As$, indicating a generation-recombination regime. At higher temperatures, an E_A lower than E_G is obtained from curve (*b*). However, this discrepancy can be removed following the correction procedure employed in Ref. 14. This subtracts the contribution of depletion layer generation and recombination at higher temperature and is performed by subtracting the extrapolated values of curve (*a*) from curve (*b*), yielding curve (*c*). This now yields an E_A of 0.67 eV, which is close to the E_G of $In_{0.53}Ga_{0.47}As$ (~0.74 eV), indicating a transition to a diffusion controlled minority carrier response. A discrepancy of ~0.07 eV is not unreasonable given that a similar deviation of E_A from E_G has been reported for a SiO_2/Si MOS device.[14] For the *p*-type device, at lower temperature curve (*d*) yields an E_A of 0.37 eV, approximately equal to $E_G/2$, indicating a generation-recombination regime. At higher temperature, curve (*f*) is obtained following the correction procedure described earlier. This yields an E_A of 0.76 eV, very close to E_G, indicating a transition to a diffusion regime. The temperature where the regime changes from generation-recombination to diffusion is known as the transition temperature (T_t). In the analysis performed for a SiO_2/Si device, this T_t corresponds with the temperature where the maximum G_m occurs,[14] which is also observed for these $In_{0.53}Ga_{0.47}As$ devices, see Fig 4 insets.

The transition frequency (f_m) is defined[14] as occurring where the capacitance in inversion is half way between the highest capacitance measured at high frequency, and the lowest capacitance measured at high frequency. A calculation of the minority carrier response time (τ_r)[14] for the devices in this study (at 295 K) yields a $\tau_{r\text{-}n}$ of 1.8 μs for *n*-$In_{0.53}Ga_{0.47}As$, and a $\tau_{r\text{-}p}$ of 51.5 μs for *p*-$In_{0.53}Ga_{0.47}As$. These correspond to transition frequencies of 25 kHz and 660 Hz for the *n*-type and *p*-type devices, respectively (open symbol plots in Fig. 1(a) and 1(b)). The transition frequency is also defined[14] as the frequency for which the measured conductance (G_m) in inversion is a maximum. For the $In_{0.53}Ga_{0.47}As$ devices in this study G_m (not shown) is also at a maximum value at the transition frequencies of 25 kHz (*n*-type) and 660 Hz (*p*-type).

In summary, a clear minority carrier response was observed for both *n*-type and *p*-type Au/Ni/Al_2O_3/$In_{0.53}Ga_{0.47}As$ MOS devices following an optimized $(NH_4)_2S$ treatment with minimal ambient exposure pre-ALD. An extraction of activation energies for the minority carrier response indicated a transition from a generation-recombination regime to a diffusion controlled response, for both *n*-type and *p*-type devices. These observations are consistent with a D_{it} which is sufficiently reduced for these *n*-type and *p*-type devices to permit the Fermi level to be swept across the $In_{0.53}Ga_{0.47}As$ band gap.

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